ABSTRACT OF THE DISCLOSURE

Operational amplifier circuits (20, 30) including error capacitors (C_3, C13) for storing finite gain effect error voltages for correction of output voltages of the circuits (20, 30), are disclosed. The circuits (20, 30) are operated in a sample clock phase to produce an approximation of the output voltage, using negative polarity versions of the input voltages to the circuit. The approximate output voltage is used to produce and store an error voltage, corresponding to the differential voltage at the input of the operational amplifier (15, 25), relative to virtual ground. This error voltage is then subtracted from the input voltage applied in the operate clock phase, to correct for the finite gain effect. A pipelined analog-to-digital converter (50) using the disclosed operational amplifier circuits (20, 30) is also disclosed.